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Total Number of Pages in This Submission

Application Number	10/061,459
Filing Date	1/31/02
First Named Inventor	Steven Teig, et al.
Group Art Unit	2825
Examiner Name	
Total Number of Pages in This Submission	Attorney Docket Number
	SPLX.P0091

Enclosures (Check all that apply)

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Signature

Date December 1, 2003

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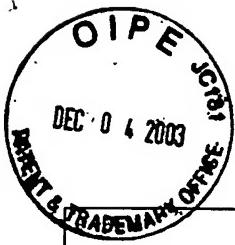
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PATENT
Docket No. SPLX.P0091

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Mari Adeli

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In the application of:

Steven Teig, et al.

Serial No.: 10/061,459

Filing Date: 1/31/02

For: METHOD AND APPARATUS FOR
PRODUCING A CIRCUIT
DESCRIPTION OF A DESIGN

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INFORMATION DISCLOSURE
STATEMENT UNDER 37 C.F.R. § 1.97

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Dear Sir:

Pursuant to 37 C.F.R. § 1.97 and § 1.98, applicants submit with this Information Disclosure Statement the attached Form PTO-1449, and copies of the documents listed in the 1449 form for consideration by the Examiner. The Examiner is requested to make these documents of record. Applicants would appreciate the Examiner initialing and returning the Form PTO-1449, indicating that the information has been considered and made of record herein.

This Information Disclosure Statement under 37 C.F.R. § 1.97 is not to be construed as a representation that: (i) a complete search has been made; (ii) additional information material to the examination of this application does not exist; (iii) the information, protocols, results and the like reported by third parties are accurate or enabling; or (iv) the above information constitutes prior art to the subject invention.

This Information Disclosure Statement is submitted within three months of the application filing date or before the mailing date of a first Office Action on the merits; accordingly, no fee or separate requirements are required.

However, in the unlikely event that the Patent Office determines that additional fees, extension and/or other relief is required, applicant petitions for any required relief including extensions of time and authorizes the Assistant Commissioner to charge the cost of such petitions and/or other fees due in connection with the filing of this document to **Deposit Account No. 50-1128** referencing SPLX.P0091. However, the Assistant Commissioner is not authorized to charge the cost of the issue fee to the Deposit Account.

Dated: December 1, 2003

Respectfully submitted,

By: _____

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DEC 04 2003 Substitute for form 1449A/PTO				Application Number	10/061,459
INFORMATION DISCLOSURE STATEMENT BY APPLICANT <i>(use as many sheets as necessary)</i>				Filing Date	1/31/02
				First Named Inventor	Steven Teig, et al.
				Group Art Unit	2825
				Examiner Name	
Sheet	1	of	1	Attorney Docket Number	SPLX.P0091

U.S. PATENT DOCUMENTS						
Examiner* Initials	Cite No. ¹	U.S. Patent Document Number	Kind Code ² (if known)	Date of Publication MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
	1.	5,519,630		05-21-1996	Nishiyama et al.	
	2.	5,537,341		07-16-1996	Rose et al.	
	3.	5,696,974		12-09-1997	Agrawal et al.	
	4.	5,574,441		05-19-1998	Tokunoh et al.	
	5.	5,787,010		07-28-1998	Schaefer et al.	
	6.	6,023,566		02-08-2000	Belkhale et al.	
	7.	6,301,696	B1	11-09-2001	Lien et al.	

NON PATENT LITERATURE DOCUMENTS		
Examiner* Initials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
	8.	Crastes, M. et al., A Technology Mapping Method Based on Perfect and Semi-Perfect Matchings, Design Automation Conference, 1991, 28 th ACM/IEEE, June 17-21, 1991, pp. 93-98.
	9.	Devadas, S. et al., Synthesis and Optimization for robustly delay-fault testable combinational logic circuits, Design Automation Conference, 1990, 27 th ACM/IEEE, June 24-28, 1990, pp. 221-227.

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